REMARKS

A Final Office Action was mailed on November 14, 2002. A response to the Final Office Action was mailed on January 8, 2003, within the two-month reply period. At that time new claims 21-25 were presented. An Advisory Action was mailed on January 29, 2003, in which new claims 21-25 were refused entry. Those claims are hereby withdrawn.

Responsive to the Final Office Action mailed on November 14, 2002, and the Advisory Action mailed on January 29, 2003, claims 1, 10, 15, and 18 are amended. New claims 26 and 27 are added. No new subject matter is added. Claims 1-20, 26, and 27 are pending. Reconsideration of claims 1-20, 26, and 27 is respectfully requested in light of the following remarks.

Claim Rejections – 35 USC § 103

1. Claims 1-20 were rejected under 35 USC §103(a) as unpatentable over applicant's prior art (APA) FIG. 1 in view of US Patent No. 5,994,732 issued to Ajika et al. ('Ajika'). The Examiner states that it would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time the invention was made to modify Applicant's FIG. 1 Prior Art by the teaching as taught in Figs. 1-3 of Ajika et al. The Applicant respectfully disagrees, and submits that the combination of Ajika and APA FIG. 1 does not teach all limitations inherent in claims 1-20 for the following reasons.

2. With respect to independent claim 1, the applicant has amended claim 1 to recite the following:

A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sectors on the substrate;

each sector comprising memory cell transistors arranged in a cell array block and decoder transistors in a column decoder block;

wherein the transistors in the cell array block and column decoder block in each sector share a common bulk region, wherein the common bulk region is formed on the substrate and is connected to a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of the sector; and

wherein said semiconductor memory device is configured to electrically erase all the memory cell transistors in a sector together.

3. Claim 1 now recites that "the common bulk region is formed on the substrate." The Examiner has previously stated that Ajika's p-well region 3 is the common bulk region (Advisory Action, page 2, part 1B). However, it is Ajika's n-well region, not the p-well region, that is formed on the substrate (FIG. 3). Thus, if Ajika's p-well region is the common bulk region, then it is not formed on the substrate as claimed. If Ajika's n-well region is the common bulk region, then all the transistors are not configured to be electrically erased together, as claimed.

4. Claim 1 also recites "wherein the common bulk region is formed on the substrate and is connected to a bulk driver *provided in each of the sectors*." Support for this amendment is found in applicant's FIG. 3. There is no evidence that the '102 reference has a bulk driver for each sector as recited by the applicants. According to Ajika, there is a well/source line driver 60a of FIG. 1 that generates a prescribed voltage to be supplied to p-well regions 3 or the source line (column 6, lines 14-21). Consequently, if Ajika's "well/source line driver" is indeed equivalent to applicant's bulk driver (which applicant disputes), then Ajika FIG. 1 teaches one bulk driver to be shared among a plurality of erase blocks. This is contrary to the recited limitation in claim 1 of a bulk driver provided in each of the sectors.

5. Claims 2-9 are allowable for at least the same reasons given above for claim 1.

6. New claim 26 is added which recites:

The device of claim 1, wherein each sector further comprises a plurality of word lines and a plurality of bit lines connecting the transistors in each sector.

New claim 26 is allowable for at least the same reasons as claim 1. In addition, claim 26 is independently allowable because Ajika's erase block does not comprise a plurality of word lines and a plurality of bit lines connecting the transistors in each sector. The Examiner has previously relied on Ajika FIG. 2 to support the statement that Ajika's erase block contains a plurality of word lines. Ajika's written description is contrary to Ajika FIG. 2, because it teaches the erase block includes "all of a plurality of memory transistors sharing *one* word line in *one* erase block 26" (column 7, lines 65-67, emphasis added).

There are other relevant portions of Ajika's written description, however, that must be considered in addition to the drawings, because the reference must be considered as a whole. *Hodosh v. Block Drug Co., Inc.* 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied,* 469 U.S. 851

(1984). The description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art. *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977).

The Examiner is relying upon Ajika FIG. 2 to show that there are multiple word lines 10 in an erase block. If this is so, then there must be only *one* bit line 24 in an erase block (FIG. 2; column 7, lines 52-59, emphasis added). There is *one* erase block in *each* p-well region (column 6, lines 1-2, emphasis added). There are *two* select gate transistors 12 provided at *either end* of every p-well region (column 6, line 56, emphasis added). *Between* the *two* select gate transistors 12, there are a plurality of memory transistors 11 that form *one* erase block (column 6, lines 56-61, emphasis added). If there are only two select gate transistors at either end of an erase block, then one of ordinary skill in the art would conclude that the plurality of memory transistors between them *must be aligned along a single bit line.* (emphasis added). Therefore, Ajika's erase block does not contain a plurality of bit lines, as does applicant's sector.

Consequently, the combination of APA FIG. 1 and Ajika fails to teach all the limitations inherent in claim 26.

7. With regard to independent claim 10, it is amended to recite the following:

A nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising:

a cell array block comprising a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of a plurality of word lines, each drain being connected to a corresponding bit line out of a plurality of bit lines;

a source line driver commonly connected to a source of each of the plurality of memory cell transistors and configured to apply a source voltage;

a column decoder block comprising a plurality of column decoder transistors, each one of the plurality of bit lines connected to one of the plurality of column decoder transistors and a common data line, the one of the plurality of column decoder transistors configured to select the each one of the plurality of bit lines;

a common bulk region arranged in each sector and formed immediately adjacent to a substrate region, wherein the plurality of memory cell transistors and the plurality of column decoder transistors in each sector share the common bulk region; and

a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of that sector.

8. Claim 10 now recites that each sector comprises a common bulk region arranged in each sector and formed immediately adjacent to a substrate region. Support for this amendment is found in applicant's FIG. 4. The Examiner has previously stated that Ajika's p-well region 3 is the common bulk region (Advisory Action, page 2, part 1B). However, it is Ajika's n-well region, not the p-well region, that is formed immediately adjacent to a substrate region (FIG. 3). Thus, if Ajika's p-well region is the common bulk region, then it not formed immediately adjacent to a substrate region as claimed.

9. Claim 10 also recites "a bulk driver provided in each of the sectors," as shown by bulk driver 400 in applicant's FIG. 3. Therefore, every sector has its own bulk driver. There is no evidence that the '102 reference has a bulk driver as recited by the applicants. According to Ajika, the well/source line driver 60a of FIG. 1 generates a prescribed voltage to be supplied to p-well regions 3 or the source line (column 6, lines 14-21). Consequently, if Ajika's "well/source line driver" is indeed equivalent to applicant's "bulk driver" (which applicant disputes), then Ajika FIG. 1 teaches one bulk driver to be shared among a plurality of erase blocks. This is contrary to the principle of every sector having its own bulk driver as recited by applicant in claim 10.

10. Claim 10 also recites that each sector comprises a source line driver. Ajika shows only a single well/source line driver 60a in FIG. 1. If Ajika's well/source line driver 60a is equivalent to applicant's claimed "bulk driver" (which applicant disputes), then Ajika does not teach a separate source line driver. If Ajika's well/source line driver 60a is equivalent to applicant's claimed "source line driver" (which applicant disputes), then Ajika does not teach a separate bulk line driver.

11. Claim 10 recites that each sector comprises a plurality of memory cell transistors and plurality of column decoder transistor sharing a common bulk region, each transistor in the common bulk region connected to one of a plurality of bit lines and one of a plurality of word lines. As explained previously in Section 6 of this paper, the combination of APA FIG. 1 and Ajika does not teach all of these elements. Thus, a *prima facie* case of obviousness is not established.

12. Claim 10 also recites *a column decoder block comprising a plurality of column decoder transistors, each one of the plurality of bit lines connected to one of the plurality of column decoder transistors and a common data line, the one of the plurality of column decoder transistors configured to select the each one of the plurality of bit lines.*

Contrary to claim 10 and as previously explained in Section 6, each of Ajika's erase blocks has only *one* bit line, and that bit line is connected to *two* column select transistors.

13 Claims 11-14 are allowable for at least the same reasons as stated above for claim 10.

14. With regard to independent claim 15, it is amended to recite the following:

A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sector units, each sector unit comprising a common bulk region, the bulk region being formed on the substrate and connected to a bulk driver, and wherein each sector unit is configured to be electrically erasable in response to an erase signal; and

a plurality of memory cell transistors and transistors of a column decoder arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage.

16. Claim 15 now recites that each sector unit comprises a common bulk region, with the bulk region being formed on the substrate. The Examiner has previously stated that Ajika's p-well region 3 is the common bulk region (Advisory Action, page 2, part 1B). However, it is Ajika's n-well region, not the p-well region, that is formed on the substrate (FIG. 3). Thus, if Ajika's p-well region is the common bulk region, then it not formed on the substrate as claimed. If Ajika's n-well region is the common bulk region, then all the transistors in the common bulk region are not configured to be electrically erasable in response to an erase signal, as claimed.

17. Claim 15 also recites that each sector unit comprises a common bulk region connected with a bulk driver. There is no evidence that the '102 reference has a bulk driver as recited by the applicants. According to Ajika, the well/source line driver 60a of FIG. 1 generates a prescribed voltage to be supplied to p-well regions 3 or the source line (column 6, lines 14-21). Consequently, if Ajika's "well/source line driver 60a" is indeed equivalent to applicant's "bulk driver" (which applicant disputes), then it is not connected to the common bulk region formed on the substrate as claimed.

18. Claims 16 and 17 are allowable for at least the same reasons as claim 15.

19. New claim 27 is added which recites:

The device of claim 17, wherein the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one.

As previously indicated in Section 6, Ajika teaches two select gate transistors at either end of each erase block. Consequently, Ajika's erase block is not equivalent to the recited sector unit structure of claim 27, and the combination of APA FIG. 1 and Ajika fails to teach

all the limitations inherent in claim 27. Thus, a *prima facie* case of obviousness is not established.

20. With respect to independent claim 18, it is amended to recite the following:

A method of forming a bulk region of a nonvolatile semiconductor device, said method comprising:

forming a bulk region for memory cell transistors provided in a cell array block of the nonvolatile semiconductor memory device, wherein the cell array block is arranged in an (M x N) array with M and N both at least equal to two; and

forming a bulk region for decoder transistors of a column decoder in the bulk region for the memory cell transistors of the cell array block, wherein the column decoder is arranged in a (P x N) array with P at least equal to one.

As previously indicated in Section 6, Ajika teaches two select gate transistors at either end of each erase block. Consequently, Ajika's erase block is not equivalent to the recited cell array block and column decoder block of claim 18, and the combination of APA FIG. 1 and Ajika fails to teach all the limitations inherent in claim 27. Thus, a *prima facie* case of obviousness is not established.

21. Claims 19 and 20 are allowable for at least the same reason as claim 18.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-20 and 26-27 of the application as amended is solicited. For the reasons explained above, the applicant believes that a prima facie case of obviousness has not been established, because the prior art does not contain all the recited elements of the independent claims 1, 10, 15, 18, 26, and 27. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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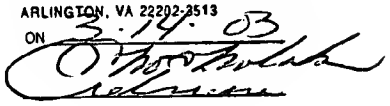

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sectors on the substrate;

each sector comprising memory cell transistors arranged in a cell array block and decoder transistors in a column decoder block;

wherein the transistors in the cell array block and column decoder block in each sector share a common bulk region, wherein the common bulk region is formed on the substrate and is connected to a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of the sector; and

wherein said semiconductor memory device is configured to electrically erase all the memory cell transistors in a sector together.

10. (Amended) A nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising:

a cell array block comprising a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of a plurality of word lines, each drain being connected to a corresponding bit line out of a plurality of bit lines;

a source line driver commonly connected to a source[s] of each of the plurality of memory cell transistors [in the cell array block] and configured to apply a source voltage;

a column decoder block comprising a plurality of [sectors, each sector comprising] column decoder transistors, [of a column decoder connected between a] each one of the plurality of bit lines connected to one of the plurality of column decoder transistors and a common data line[s], the one of the plurality of column decoder transistors configured to select the each one [bit line out] of the plurality of bit lines; [and]

a common bulk region arranged in each sector and formed immediately adjacent to a substrate region, wherein the plurality of memory cell transistors and the plurality of column decoder transistors [of] in each sector share the common bulk region; and

a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of that sector.

15. (Amended) A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sector units, each sector unit comprising a common bulk region, the bulk region being formed on the substrate and connected to a bulk driver, and wherein each sector unit is configured to be electrically erasable in response to an erase signal; and

a plurality of memory cell transistors and transistors of a column decoder arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage.

18. (Amended) A method of forming a bulk region of a nonvolatile semiconductor device, said method comprising:

forming a bulk region for memory cell transistors provided in a cell array block of the nonvolatile semiconductor memory device, wherein the cell array block is arranged in an (M x N) array with M and N both at least equal to two; and

forming a bulk region for decoder transistors of a column decoder in the bulk region for the memory cell transistors of the cell array block, wherein the column decoder is arranged in a (P x N) array with P at least equal to one.

26. (New) The device of claim 1, wherein the cell array block and the column decoder block of each sector share a plurality of word lines and a plurality of bit lines.

27. (New) The device of claim 17, wherein the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one.